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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/681,206	10/09/2003	Mototsugu Fuji	HITA.0441	8330

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REED SMITH LLP
3110 FAIRVIEW PARK DRIVE, SUITE 1400
FALLS CHURCH, VA 22042

EXAMINER	
JACOB, MARY C	
ART UNIT	**PAPER NUMBER**
2123	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/681,206	FUJI ET AL.	
	Examiner	Art Unit	
	Mary C. Jacob	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S C. § 133). Any reply received by the Office later than three months after the mailing date of this communication even if timely filed may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 2-7 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 2-7 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The response filed 1/5/07 has been received and considered. Claims 2-7 are presented for examination.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: page 23, line 6; page 28, lines 3 and 22; page 31, line 4 refer to elements 0029-0032, however, it may have been intended to reference elements 0028-0031 in Figures 10, 12, 13. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities. The specification appears to be a direct translation from a Japanese document and contains numerous grammatical errors, for example: Abstract, line 3, "wired in direct between";

page 2, line 3, "may be varies"; page 2, line 15, "separates into the portion to realize the logic"; page 4, lines 3-7, "direction control signal of two way signal". Applicant's assistance is requested in correcting the grammatical errors throughout the specification.

4. A substitute specification in proper idiomatic English and in compliance with 37 CFR 1.52(a) and (b) is required. The substitute specification filed must be accompanied by a statement that it contains no new matter.

Claim Objections

5. The objections to the claims recited in the Office Action dated 7/12/06, not repeated below, have been withdrawn in response to the amendments to the claims filed 1/5/07.

6. Claim 2, line 13, "in direct" would be better if written, "directly".

7. Claims 5 and 7 appear to be repetitive.

8. Claims 5 and 7 recite "giving the priority in determination of signal direction to one of the EPGA module and the bridge circuit having higher drivability". The claim language is unclear and should be revised for clarity.

Claim Rejections - 35 USC § 112

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. The rejections of the claims under 35 U.S.C. 112, second paragraph, recited in the Office Action dated 7/12/06, not repeated below, have been withdrawn in response to the amendments to the claims filed 1/5/07.

11. Claims 2-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

12. Claims 2-7 contain various recitations of "EPGA" and "FPGA". It is unclear whether "EPGA" is intended to read, "FPGA". This also leads to examples wherein there is a lack of antecedent basis in the claims (for example, Claim 2, line 9, "said FPGA module" and "said EPGAs"). Further, it is noted that there is no recitation of "EPGA" in the specification.

13. Claim 3 recites "the verification logic implemented on said FPGA module". Claim 2 recites that "a verification logic...is assigned to an external interface connector of the FPGA module". Therefore, it is unclear how "the verification logic" is "implemented" on the FPGA module since Claim 2 contains no recitation of the verification logic being "implemented" on the FPGA module.

14. Claim 6 recites "a signal direction of the FPGA module" in line 7. It is unclear whether this is a new limitation of a "signal direction" or if this refers to the "signal direction" "between said FPGA module and the bridge circuit" that is input to the logic simulator in lines 4-5.

Claim Interpretation

15. "EPGA" recited in Claims 2-7 was interpreted to read, "FPGA".

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 2-7 are rejected under 35 U.S.C. 103(a) as being obvious over Evans et al (US Patent 6,279,146) in view of Fuji et al (US Patent 6,564,367).

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

18. As to Claim 2, Evens et al teaches: a logic verification system comprising:

a logic simulation accelerator (column 9, lines 60-67; column 10, lines 18-24) including:

a logic simulator operating on a general purpose processor (Figure 2, element 86, 118);

a device including a programmable FPGA module composed by FPGAs (Figure 2, element 60 and included elements; column 9, lines 3-11); and

a bridge circuit which selectively transmits and receives corresponding data between said logic simulator operating on said general purpose processor and said FPGA module according to designed functions assigned to said FPGAs for each of a plurality of designed logic circuits (Figure 2, element 72; column 9, lines 29-62)

wherein all pins of the FPGA module used in a verification process for verifying one of said plurality of designed logic circuits by said logic simulator are wired to the bridge circuit to accelerate logic simulation (column 9, lines 32-43; column 9, lines 60-67; column 10, lines 18-24).

19. Evans does not expressly teach: wherein all the pins of the FPGA module are wired directly to the bridge circuit; a cutting end of a verification logic of said one of the plurality of designed logic circuits is assigned to an external interface connector of the FPGA module; and a correspondence between each pin of the external interface connector of said FPGA module and a logic signal is established on said logic simulator on said general purpose processor.

20. Fujii et al teaches a logic dividing and module wiring system wherein according to the logic dividing method, associative relations determining assignments of external interface signals of logic to connector pins is acquired in advance, and using this information, pieces of logic related to the external interface signals are assigned to

FGPAs which are wired to connector pins on a 1 to 1 basis and a result, an external interface signal does not pass through an unrelated FPGA along a path starting from a connector pin and ending at an FPGA to which the logic related to the external interface signal is assigned, therefore, the logic emulation can be carried out at a high speed (column 4, line 66-column 5, line 11). The method taught by Fuji et al teaches a module contains FPGA devices implementing logic for verification (column 3, lines 61-64; Figure 3; Figure 6, "Type A" and description), a module connector for electrically connecting the module to an external device (column 3, lines 66-67; Figure 6 and description), wherein all the pins of the FPGA module are wired directly to the connector to accelerate emulation (column 4, line 66-column 5, line 11); a cutting end of a verification logic of said one of the plurality of designed logic circuits is assigned to an external interface connector of the FPGA module (column 6, lines 64-66; column 7, lines 44-48); and a correspondence between each pin of the external interface connector of said FPGA module and a logic signal is established (column 7, lines 44-48; Figure 5 and description).

21. Evans et al and Fujii et al are analogous art since they are both directed to accelerating logic operations that verify a logic design programmed a plurality FPGAs wherein the module containing the FPGA devices is connected to an external device.

22. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the logic verification system as taught by Evans et al to further include the direct wiring of the FPGA module to the bridge circuit like the direct wiring of the FPGAs to the external connectors as taught in Fujii et al, wherein a cutting

end of a verification logic of said one of the plurality of designed logic circuits is assigned to an external interface connector of the FPGA module and establishing a correspondence between each pin of the external interface connector of said FPGA module and a logic signal on the logic simulator, since Fujii et al teaches a logic dividing and module wiring system wherein pieces of logic related to the external interface signals are assigned to FGPAs which are wired to external connector pins on a 1 to 1 basis resulting in logic emulation carried out at a high speed (column 4, line 66-column 5, line 11).

23. As to Claim 3, Evans et al in view of Fujii et al teach: wherein the verification logic implemented on said FPGA module is provided with means for transmitting a direction control signal of a two-way signal controlled therewith to the bridge circuit using an interface (Evans et al: column 5, lines 40-47; column 13, lines 6-9; lines 25-28).

24. As to Claim 4, Evans et al in view of Fujii et al teach: the logic verification system further comprising means for automatically detecting a signal direction of a two-way signal between said FPGA module and the bridge circuit (Evans: column 5, lines 40-56; column 13, lines 25-28), and the program data of the same FPGA module implementing different verification logics used in verification processes consisting of acceleration of logic simulation and logic emulation for the plurality of designed logic circuits (Evans et al: column 8, line 66-column 9, line11; column 10, lines 18-24; Fujii et al: Figure 1, element 101; column 4, line 66-column 5, line 9).

25. As to Claims 5 and 7, Evans et al in view of Fujii et al teach: wherein said means for automatically detecting the signal direction of the two way signal sets a drivability level of output circuits of the FPGA module and the bridge circuit and giving a priority in determination of signal direction to one of the FPGA module and the bridge circuit having higher drivability (Evens et al: column 5, lines 40-47; column 13, lines 25-28; column 13, line 47-column 14, line 25).

26. As to Claim 6, Evans et al in view of Fujii et al teach: means for inputting the signal direction of the two-way signal to the logic simulator on the general purpose processor, wherein a disagreement between a signal direction of the logic simulator and a signal direction of the FPGA module is detected by comparing said signal directions (Evans et al: column 13, lines 25-28; column 14, lines 26-49).

Response to Arguments

27. Applicant's arguments filed 1/5/07 have been fully considered but they are not persuasive. Applicant's argues, "the cited references do not teach or suggest a logic simulator + FPGA module logic verification scheme which includes a logic simulation program operating on a general purpose processor working in conjunction with a programmable FPGA module composed by FPGAs and a bridge circuit with selectively transmits and receives corresponding data therebetween" (page 5). These arguments are in regards to limitations that have been amended into the claims and are addressed in the claim rejections above.

Conclusion

28. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

29. Rajsuman et al (US Patent 6,678, 645) teaches a method and apparatus for verifying system on a chip designs that includes FPGA emulation and an interface circuit for interfacing between the verification unit and the IC being tested.

30. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary C. Jacob whose telephone number is 571-272-6249. The examiner can normally be reached on M-F 7AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mary C. Jacob
Examiner
AU2123

MCJ
3/8/07

PAUL RODRIGUEZ
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

3/9/07